CHIP DESIGN
COMPETITION SPECIFICATIONS

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CHANGE TRACKING TABLE

VERSION	DATE	CHANGE PLACE	DESCRIPTION
V1	18.02.2022		First publication
V2	23.03.2022	2.4.1, 2.4.2, 3.2.1, APP-3	Changes were made to the design requirement and test descriptions were added

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ABBREVIATIONS

ADC: Analog-to-Digital Converter
BİLGEM: Informatics and Information Security Research Center
BP: Band Pass
DC: Direct Current
DDK: Advisory and Evaluation Board
DEF: Design Exchange Format
DRC: Design Rule Check
DRV: Design Rule Violation
DSP: Digital Signal Processing
DDR: Detailed Design Report
FPGA: Field Programmable Gate Array
GDS: Graphic Data System
HDL: Hardware Description Language
IIP3: Input Third Order Intercept Point
IRN: Input Referred Noise
ISA: Instruction Set Architecture
KYS: Enterprise Management System
LNA: Low Noise Amplifier
LTE: Long Term Evolution
LVS: Layout versus Schematic
PDR: Preliminary Design Report
PSRR: Power Supply Rejection Ratio
PTK: Process Design Kit
RISC: Reduced Instruction Set Architecture
RF: Radio Frequency
RTL: Register Transfer Level
SDF: Standard Delay Format
SPI: Serial Peripheral Interface
T3 Foundation: Turkey Technology Team Foundation
TT: Typical- Typical
TÜBİTAK: Scientific and Technological Research Council of Turkey
UART: Universal Asynchronous Receiver Transmitter
WIPO: World Intellectual Property Organization

1 PURPOSE

The Chip (Integrated Circuit) Design Competition, which will be opened to university students for the first time in 2022 within the scope of TEKNOFEST, aims to raise awareness in the field of micro-electronic technologies in associate, undergraduate and graduate (master) students and to provide students with knowledge on IC design. The competition is also organized to encourage teamwork and to lead the formation of competent human resources in this field by developing micro-electronic technologies with practical applications.

This document has been created to define all the rules and requirements of the Chip Design Competition, which is organized by the TÜBİTAK BİLGEM Integrated Design and Education Laboratory (TÜTEL) within the scope of TEKNOFEST Aviation, Space and Technology Festival (TEKNOFEST) Technology Competitions.

2 GENERAL INFORMATION ABOUT THE COMPETITION

The competition consists of two categories; analog and digital. Designing a customized processor with RISC-V Instruction Set Architecture (ISA) is expected in the digital design category. Designing a 4th order active low-pass filter is expected in the analog design category.

What is expected from the teams that will participate in the competition is to prepare the preliminary design report, detailed design report, complete the design, prepare the design outputs and make a presentation/demo in the final for the hardware that meets the design criteria specified in this document.

Applications will be made through the official website of TEKNOFEST Technology Competitions (www.teknofest.org) until March 14, 2022.

2.1 Participation Rules

- Higher education (associate, undergraduate and master graduate) students studying in Turkey can participate in the competition.
- Participation in the competition can be made individually or as a team. Teams must consist of a maximum of 4 people. Apart from this, teams can only take 1 person as a consultant.
- Along with the Detail Design Report, approved student documents must be submitted for students, and a certified document showing that they are a lecturer/staff or research assistant for advisors.
- Teams can be formed from a single school or as a mixed team with one or more higher education students coming together.
- Each team participating in the competition can participate in the competition with a maximum of one design.
- Competitors who have completed the team formation process must apply to the competition in accordance with their project.
- Between the application dates, the team captain/advisor registers through the system, makes the correct and complete registration of the consultant and/or team captain/team members, if any, and sends an invitation to the advisor and members' e-mails, if any. The member to whom the invitation is sent, logs in to the Application system, accepts the invitation from the "My Team Information" section and the registration is completed. Otherwise, the registration will not be completed.
- All necessary processes within the scope of the competition (Application, Report Receive, Report Results, Financial Support Application, Objection Processes, Member addition/removal

procedures, etc.) are done through the KYS system. Teams are required to follow their processes through the KYS system.

- Adding/removing members is done until the Detail Design Report Submission date.
- During the competition process, the processes of applying through the KYS, uploading reports and filling out forms are under the authority of the team captain and/or the consultant, and the competition processes are managed through these people.
- Transportation and accommodation support to be provided to the finalist teams is limited. The number of people to be supported is 3 people (including the consultant) per team and TEKNOFEST Competitions Committee has the right to make changes.
- TEKNOFEST Competitions Committee has the authority to limit the number of members in the festival area. In case of restrictions, the committee will inform.
- During the competition process, your education level at the time you applied will be taken into account. You should pay attention to this when choosing a category.
- Applications of TÜBİTAK BİLGEM employees will not be evaluated.

2.2 Competition Schedule

Table 1: Competition Schedule

DESCRIPTION	DATE
Competition Application Deadline	14.03.2022
Preliminary Design Report Deadline	11.04.2022
Announcement of the Teams Passing the Pre-selection Based on the Results of the Preliminary Design Report (PDR)	22.04.2022
Giving Integrated Circuit Design Training to the Teams Passing the Pre-selection	14.05 .2022 - 15.05.2022
Detail Design Report (DDR) Deadline	20.06.2022
Announcement of Finalist Teams	27.06.2022
Deadline for Final Presentations	10.08.2022
Final Evaluation Presentations	15.08.2022 - 18.08.2022
TEKNOFEST	30.08.2022 - 04.09.2022

2.3 Reports and Presentation

- Citation format can be accessed under the heading of general rules in the specification.
- Two reports, a preliminary design and a detail design report, will be submitted. The technical information required in the relevant headings of the reports should be conveyed in detail.
- Report templates are published on the competition website.

- Reports can be prepared in Turkish or English. It is mandatory to use a single language in all report content.
- The reports are uploaded to the application system in PDF format with a maximum size of 60 MB until the specified deadlines. Otherwise, the team will be eliminated from the races.
- The reports should be prepared in A4 format, 11 point, Calibri font, with a line spacing of 1.15 and 2.5 cm at the bottom, top and sides. The preliminary design report should have a maximum of 6 pages, and the detailed design report should have a maximum of 20 pages (including the cover page, pictures, tables, references).
- The report is evaluated within the scope of scientific and technical criteria specified by DDK members who are experts in their fields. The score of the team is determined by summing the points of all DDK members. Teams that score below the score to be determined by TÜBİTAK are eliminated from the race.
- Teams with successful reports are announced on the www.teknofest.org page.
- In case of an ethical violation such as plagiarism, copying etc., the report will not be evaluated and the corresponding team will be eliminated from the competition. This rule is applied for the application of the same university/club/society etc. regardless of category/race.
- Objections to the report score results can be made through the KYS system within five (5) business days following the announcement of the relevant results. Objections are evaluated by DDK and the results are notified to the teams by e-mail.

2.3.1 Preliminary Design Report (PDR)

Preliminary design report is expected to include the following sections:

Block diagram of the overall design, target performance summary table, system level importance of targeted performance measures, schematics of the possible critical circuit core, brief description of the circuit and design techniques to be used, applicable references (e.g., an article that inspires your design, all the open-source blocks you'll reuse, etc.).

The up-to-date report template will be shared on the competition website.

In order to proceed to the next stage within the scope of this competition, the preliminary design report must be submitted and deemed successful. Teams deemed successful in the preliminary design phase will be entitled to receive training on the installation and use of the IC design environment. Training details will be announced on the competition website. No evaluation will be made as a result of the training, and all teams are responsible for preparing a detailed design report.

2.3.2 Detailed Design Report (DDR)

In the analog category detailed design report, it is expected that the schematic level design will be completed and reported with the results.

In the detailed design report of the Digital Design category, the details of the realized design, how the problems presented in the specification were handled, block diagrams, simulation and synthesis results should be included.

The up-to-date report template will be shared on the competition website.

Teams that have passed to the DDR stage are obliged to submit their reports on the date specified in Table 1.

According to the DDR results, the teams that will participate in the final evaluation will be announced on the date specified in Table 1.

2.3.3 Final Evaluation Presentation and Design Outputs

Final evaluation presentation and design outputs (schematic, RTL, GDSII etc.) must be submitted by the date specified in Table 1. Using the design outputs, the results in the presentation will be verified and the non-conforming groups will be eliminated. For this reason, the design outputs must be up-to-date and compatible with the presentation. Details of the design outputs are given in Section 3.3.

2.4 Evaluation

Teams that pass the PDR stage will be entitled to participate in the DDR stage. Teams that pass the DDR stage will be eligible to participate in the presentation evaluation. Preliminary design and detail design reports will be evaluated in accordance with the template to be announced on the competition page. First, second and third competitors will be determined based on the final presentation/demo. Presentation evaluation will be made by the competition jury according to the oral presentation and the answers to the questions of the evaluators.

2.4.1 Digital Design Category

Evaluation consists of several stages. Firstly, the processor (RV64IMCX instruction set processor, UART and SPI peripherals) requested from the competitors will be put into a test environment, and the interface of the processor should be compatible with the wrapper module that will be shared with the competitors. Test codes will be loaded into the main memory located in the top module wrapper in a shuffled manner. In this test environment, it will be tested whether or not the competitor implements the instruction set correctly. During the tests, some boundary conditions (such as dividing a number by zero) will also be tested. For testing the UART and SPI blocks, commands will be sent to these blocks over the peripheral bus in accordance with the register address space given in APP-3. Secondly, these blocks will be tested with the processor first in the simulation environment, then on the FPGA (Nexys A7 XC7A100T-1CSG324C).

Projects that have been tested and found to work correctly will be subjected to performance analysis. In this analysis, various performance tests (e.g., CoreMark) will be run on the processor. A final score will be obtained using the values from the tests. Scoring will be made out of 100. Demo with reports and presentation will be evaluated out of 100 points in itself. Of the total score, 50% will be reports, 10% will be performance criteria, and the remaining 40% will be demo with presentation.

The total score that can be obtained at the end of the competition will be a maximum of 100 points and the calculation will be made as follows.

Total Points = (0.15 * PDR Points) + (0.35 * DDR Points) + (0.40 * Presentation and Demo Points) + 10 Performance Criteria Points - Penalty Points

10 Performance Criteria Points will be awarded as follows: the team with the lowest space usage as a result of chip flow 2 points, the team with the lowest power consumption 2 points, the team with the highest performance (clock frequency x IPC – instructions per second) 2 points, and when these three criteria are considered together, the team with the most successful PPA (Power-Performance-Area) will get 4 points. The team that meets all of the mentioned criteria will receive 10 points. Penalty points will be calculated and deducted from the total score for each non-applied item from the requirements that are not included in the minimum success criteria. After the chip flow, the projects that meet the

minimum criteria will be ranked according to the scoring and the top three teams will be determined. In the event of a tie, the team with the least penalty points will take the lead in the ranking.

2.4.2 Analog Design Category

Scoring will be made out of 100-point and, reports and presentations will constitute the entire score. Of the total score, 40% will be reports, 10% will be performance criteria, and the remaining 40% will be presentation. In the analog design category, evaluation will be made through post-layout simulations.

The total score that can be obtained at the end of the competition will be a maximum of 100 points and the calculation will be made as follows.

Total Score = (0.15 * PDR Score) + (0.35 * DDR Score) + (0.25 * Presentation) + (0.25 * Performance Criteria Score)

Performance Criteria Scores will be considered as the sum of the scores of the filter and bandgap reference voltage circuits and according to the following criteria be evaluated:

- Lowest power consumption and layout area utilization (filter and bandgap reference voltage circuit)
- Highest linearity and lowest noise values (filter)
- Highest attenuation rate (filter)
- Lowest temperature coefficient (bandgap reference voltage circuit)
- Lowest PSRR (bandgap reference voltage circuit)

The design that provides the highest rate of these criteria will earn 30-point performance criteria score.

2.5 Contact

For technical questions about the contest, communication will be made via the mail group. It is the responsibility of the competing team to actively follow this group and to follow the announcements and questions & answers in this group. Referees and jury committees are not responsible for the failure of the teams to reach up-to-date information as a result of not following the specified e-mail group.

Questions about the organizational parts of the competition should be submitted via iletisim@teknofest.org e-mail address.

It is important that your technical and organizational questions are conveyed through the correct channels above, in order to be able to respond quickly to the questions asked.

3 TECHNICAL RULES

3.1 Design Environment and Technology

In the digital design category, Verilog-2005 hardware design language (HDL) must be used for the hardware to be developed. The rules given in section APP-5 must be followed while writing the Verilog code. The design must be updated at least every two months to a private repository opened on GitHub and shared with the competition evaluation board. In the chip design phase, OpenLane flow and open source PDK of Skywater 130nm technology should be used. Post IC flow evaluations will be done at TT (Typical-Typical) – 25 C – 1.80V corner.

In the analog design category, open-source design tools (Xschem, Magic, Ngspice and Netgen) and Skywater 130 nm technology will be used. The designs will be updated to a special repository created on GitHub before the delivery of the detail design report and final presentation and will be shared with the competition evaluation board.

3.2 Design Requirements

3.2.1 Digital Design Category

In the digital design category of the competition, a customized processor with the RV64IMCX Instruction Set Architecture is expected to be designed. During the processor design phase, the constraints specified in Section 3.1 must be complied with. Participants can reuse circuits available within the open-source design community (appropriate references should be provided).

The features that the processor in question should have are listed below.

- Support for the instructions given in APP-1
- Support for special instructions specified in APP-2
- Supporting UART and SPI peripherals detailed in APP-3
- In the addition process, the *ripple-carry* adder and addition symbol ("+") are not used, but are replaced by another addition algorithm
- In the multiplication process, the multiplication symbol ("*") is not used, but another multiplication algorithm is used in its place
- In the division process, the division symbol ("/") is not used, but is replaced by another division algorithm
- 2 KB level 1 instruction cache (L1 Instruction Cache) inside the fetch stage
- Load-Store unit has 1st level data cache (L1 Data Cache) with size of 2 KB
- 8 KB level 2 cache (L2 Cache) for data that is not in level 1 caches
- 32-bit off-chip interface in the processor design for data that is not in level 2 cache (Signals in the interface and the specifications of the transfers will be determined in the top module(wrapper) to be shared by the competition committee.)
- This interface should be used for data from the end address of the peripherals to the end address of the main memory, and data outside the main memory region should be forwarded to the processor without storing into caches
- Only the data between 0x40000000 and 0x40080000 addresses should be cacheable
- The program counter value at boot time should point to the base address of the main memory
- Cacheable data and instructions should be stored in memory in a shuffled manner as specified in APP-4 to prevent data theft from the memory

3.2.2 Analog Design Category

Increasing communication habits of our age lead communication systems to be lower cost, compact, efficient and fast. Transceiver circuits developed in this direction are also implemented in integrated circuits (integrated circuit, chip) instead of discrete elements in order to meet the increasing performance demand.

Figure 1 shows a direct-conversion receiver architecture. After the signal coming to the antenna is filtered and amplified with a low-noise amplifier, it is down-converted to the baseband with a mixer. After the baseband signal is cleared of out-of-channel signals by passing it through a low-pass filter, it is converted into a digital signal with the help of an analog-to-digital converter and processed.

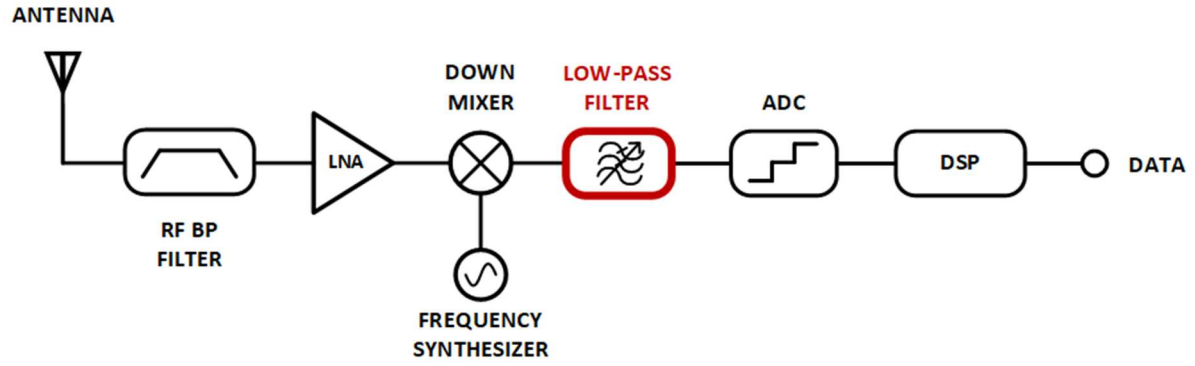


Figure 1 : Direct Cycle Receiver Architecture

LTE (Long-Term Evolution) standard is a current communication standard that we commonly use in mobile communication. A channel in the LTE standard can have a wide range of bandwidths (1.4, 3, 5, 10, 15, 20 MHZ). The appropriate bandwidth is selected according to the communication density and device support.

Designers are requested to design a baseband analog low-pass filter for the LTE standard transceiver. The filter to be designed within the scope of this competition will only support 10 MHz and 20 MHz channels and will have a 4^{th} order Butterworth transfer function. In addition, it is expected to design the bandgap reference circuit required for the biasing of the filter. In Figure 2, the blocks to be designed within the scope of the competition are visualized.

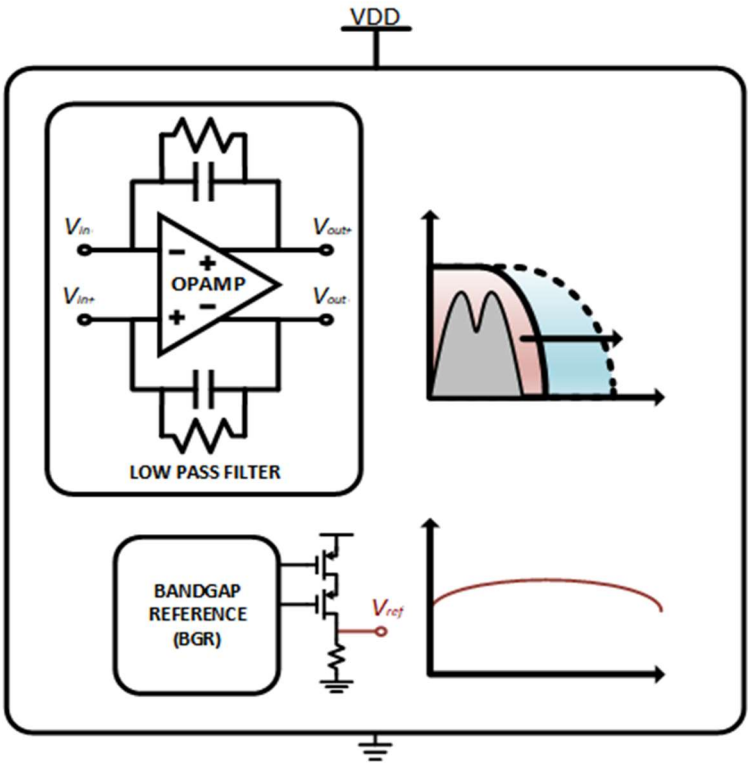


Figure 2: Block Diagram of Filter and Bandgap Reference Voltage Circuits

Block level and general design requirements are given below in detail.

General Requirements:

- The design environment and technology specified in Section 3.1 must be complied with.
- All circuits should be powered by only one ideal voltage source of 1.8 V.
- All circuit elements should be used from the Skywater 130nm library, ideal elements should not be used.
- Simulations should be made at the TT (Typical-Typical) process corner and at 27°C. The 27°C temperature is the nominal temperature at which the entire design will operate. Only simulations of the bandgap reference voltage circuit should cover the temperature range of -40°C to 125°C.
- Verify that the following requirements are met by post-layout simulations.
- The schematic and post-layout simulation results should be presented comparatively.
- Except for start-up circuits, all MOS transistors must operate in the saturation region.
- Stability analysis should be performed when necessary.

Filter chip requirements:

- There should be 2 different programmable cut-off frequencies, 10 MHz and 20 MHz.
- The frequency response should be a 4th order Butterworth filter convergence. The filter should have a minimum attenuation rate of 70 dB at the 10 times of the cutoff frequency.
- Active-RC filter topologies should be used.
- The DC gain should be constant 10 dB.
- For each cutoff frequency, the minimum IIP3 (third order input intercept point) and IRN (input-referred noise) values should be 15 dBm and 100 nV/$\sqrt{Hz}$. In addition to the IIP3 value, the input P1dB value should also be simulated and presented.

- The differential output swing range should be between 0 V-2.2 V.
- The maximum power consumption should be 60 mW.
- Above requirements must be verified while the filter is biased with reference currents generated from the bandgap reference circuit.
- The group delay must be displayed for each cutoff frequency of the filter.

Operational amplifier requirements to be used in the filter:

- It must be fully-differential.
- It should have a minimum DC gain of 70 dB, a minimum phase margin of 60 degrees for a differential capacitive load of 2 pF, and a gain-bandwidth product of 2 GHz.
- The input & output common-mode voltage should be set to half of the supply voltage.

Bandgap reference voltage circuit requirements:

- A 300 mV reference voltage should be generated as shown in Figure 2 for the purpose of validating the bandgap reference circuit.
- The reference voltage should vary by a maximum of 20 ppm/°C, covering the temperature range of -40°C to 125°C.
- For 1.8±10% supply voltage, the 300mV reference voltage should not change and the transistors should protect their nominal operating regions.
- A start-up circuit should be utilized to avoid circuit startup problems.
- The PSRR value should be below 0 dB in the 1 Hz-10 GHz range.

3.3 Design Outputs

Digital design category: The expected design outputs for the digital design category are listed below. All these outputs can be generated via OpenLane. The files given below must be reproducible through the design in the repository created by the competitors on GitHub.

- GDSII (.gds): The industry standard layout file format used for submitting the design to production. DRC (Design Rule Check) will be performed by reading GDSII (Graphic Design System) via Magic. With Netgen, LVS (Layout versus Schematic) will be made.
- Gate level netlist after layout (.v): The gate level netlist shows the standard cells and their connections in the design obtained after the chip flow. By using the gate level during the simulation, it will be verified that the design gives the correct outputs against the given inputs even after the chip flow.
- SDF (Standard Delay Format): SDF refers to the delay information of standard cells and the connections between them.
- DEF (.def): The DEF (Design Exchange Format) file contains the location of standard cells in addition to the port level netlist. By reading over the Klayout program, general examinations about the design will be made and field information will be obtained.
- Reports: The design needs to be clean in terms of timing (setup, hold), DRV (maximum capacitance, max fanout (should not exceed 5), max slew), and physical verification (DRC, LVS, antenna control). For this purpose, test/analysis reports should be given.

The expected design outputs for **analog design category** are as follows:

- GDSII (.gds) (GDS: Graphic Design System): The industry standard layout file format used for submitting the design to production. It will be used for layout evaluation and physical verifications (DRC/LVS).

- Design and test environment schematics (.sch): These are the files created by Xschem that contain the transistor-level designs and the test environment related to these designs. All schematic files used in the project should be included in the printouts to validate my designs.
- Schematic and post-layout transistor level netlist (.spice): The transistor level netlist is the file showing the PTK elements in the design and their connections with each other. In the post-deployment netlist, parasitic elements are also included in this file. This file will be used for pre- and post-layout performance verifications.
- Layout output files (.mag): Magic layout program output file. It is requested for the control of the layout.
- Physical Verification Reports: It consists of reports containing the results of physical verification tests (DRC/LVS).

4 AWARD

As a result of separate evaluation in three stages, the teams that pass the report stages, reach the finals in their own category, meet the award criteria, and are ranked in the final evaluation, will be awarded a monetary award as indicated in Table 2 and Table 3. Analog and digital categories will be evaluated and awarded separately. First, second and third place awards will be divided equally according to the total number of team members (all members registered in the system) and will be deposited into the bank account specified by each person.

Table 2: Analog Category Awards

GRADE	AWARD AMOUNT	CONSULTANT
First	40.000 ₺	2.000 ₺
Second	30.000 ₺	2.000 ₺
Third	20.000 ₺	2.000 ₺

Table 3: Digital Category Awards

GRADE	AWARD AMOUNT	CONSULTANT
First	40.000 ₺	2.000 ₺
Second	30.000 ₺	2.000 ₺
Third	20.000 ₺	2.000 ₺

4.1 Minimum Success Criteria for Award Ranking in the Digital Design Category

The minimum success criteria that competitors must meet in order to enter the award ranking are as follows:

- The processor must support all 64-bit instruction extensions in this document.
- The checks specified in the Design Outcomes Section (3.3) should be performed to show that there are no violations.
- The processor must successfully complete any software to run on it during testing.
- Design files should be available in GitHub repository and updated every 2 months.

In addition, the competitor must have passed the presentation stage and must be in the festival area on the day of the event.

4.2 Minimum Success Criteria for Award Ranking in The Analog Design Category

The minimum success criteria that the competitors must meet in order to enter the award ranking are as follows:

- Functional operation of the filter and bandgap reference circuit must be correct.
- The bandwidth, gain, attenuation rate requirements of the filter must be met for post-layout.
- Gain-bandwidth product requirement of OPAMP must be met for post-layout.
- The temperature coefficient and PSRR requirements of the bandgap reference circuit must be met for post-layout.

Also, the competitor must have passed the presentation stage and be in the festival area on the day of the event.

5 GENERAL RULES

- Authorized persons of each team have the right to appeal to the relevant referee. Objections can be made verbally, provided that they are submitted in writing later. Verbal objections are made in writing within 24 hours at the latest. In any case, unwritten objections will not be taken into consideration. Objections are examined by the referee committee and resolved within 7 workdays.

- After the evaluation results are announced, authorized people from each team are required to submit their objections and justifications in writing. Objections submit from www.t3kys.com website.
- Objections must be submitted from the date the competition results until committee specified date announced. Otherwise, the objections are not taken into consideration.
- The assignment of the advisor; to help students to plan their own education, to guide them in academic, social and cultural issues, contribute to development of the student's personality as a whole with its mental, social and emotional aspects, etc. tasks and services. The role of the advisor in the team is to provide the academic support that will be needed in the project, to guide the team members to find solutions to their problems.
- Although the subject of the competition is the result of the effort of the competitor/competitors in the team, the intellectual work reflects the characteristics of the team members and the Advisor will not be accepted as the owner of the work.
- Teams that have benefited from the past years reports on website should indicate on the relevant page that they quoted. You must state the explanation after the quoted sentence. QUOTE FORMAT: "Cited Sentence/s" (Year, Competition Name, Category, Team Name) EXAMPLE CIRCUMSTANCE: "The most important problem that slows down the debris removal and earthquake victim search efforts is that the location of the earthquake victim is not determined in the debris." (2020, Technology Contest for the Benefit of Humanity, Disaster Management, Team X)
- Each competitor is obliged to take the necessary safety precautions while racing and to show the expected attention to his environment.
- Turkey Technology Team (T3) Foundation and the organizing committee, to take place in objective criteria of the competition terms can lead to fair results, competitors can be better met their every need, ensuring the safety measures and order becomes effective competition conditions reserves the right to make any changes in the present specification.
- T3 Foundation and the organizing committee reserve the right to cancel the competitions in the event that there are not enough applications with the technical
- knowledge and skills required to participate in the competitions as a result of the evaluations to be made after the application process.
- TEKNOFEST Safety and Security Specifications are notified to all competitors, delegations and relevant persons. All teams that will compete within the scope of the organization are obliged to meet the safety conditions specified in the TEKNOFEST Safety and Security Specification, specific to the competition they compete. In this respect, it is the competitors' responsibility to take additional precautions arising from the systems used, other than those included in the said safety instruction.
- T3 Foundation and the organization committee reserve the right to exclude teams that are found to not meet the conditions specified in the TEKNOFEST Safety and Security Specifications in order to ensure that the organization can be held in a safe environment. T3 Foundation and organization officials are not responsible for any damages that may occur as a result of the violations of the competitors, delegations and related person during the competition.

- Concerning the competition, the competitor accepts and undertakes all kinds of written or visual promotions, publications, social media and internet broadcasts to be made before or after the competition by the T3 Foundation and/or TEKNOFEST. In addition, the competitor is entitled to the rights of processing, dissemination, reproduction, representation, visual or auditory means and the right to transmit to the public on the designs, codes and scientific and artistic work produced or contributed to the production of T3 Foundation/TEKNOFEST without any time limitation. e, accepts, declares and undertakes that he consents to the presentation of the relevant work to the public within the framework of the open source policy of the T3 Foundation and its use and development by the relevant persons by reference. T3 Foundation reserves the right to make changes on the work when necessary and to make all intellectual property available to the public (limited to what it shares with the T3 Foundation) as and when it deems appropriate.
- Concerning the rights of the competitor on the part of the work transferred to the T3 Foundation, a registration can be made with the Turkish Patent and Trademark Office or WIPO (World Intellectual Property Organization) within the framework of the Industrial Property Law No. 6769 and other legal regulations governing Intellectual Property Rights, provided that the written permission of the T3 Foundation is obtained or to apply for protection, that T3 Foundation and T3 Foundation will not prevent its use by applying any prohibition against third parties who benefit within the scope of open source code policy with the knowledge of the T3 Foundation, will not apply for protection measures within the scope of legal legislation, and will not request for stopping the use with the claim of violation, and commits.
- In the event that the T3 Foundation and TEKNOFEST suffer damage due to the violation of the intellectual and industrial property rights of any product, the said damages will be covered by the relevant team (including the advisor).
- A Participation Certificate will be given to all finalist teams that qualify to participate in the competition.

6 CODES OF CONDUCT

In the festival area or during the competition process (report stages, evaluation process, etc.) a situation, action, speech, etc. that is against public morality. Behavior that actual performers at the moment when detected / person to start the legal process urgently about and the team has at least 2 years during operations in Turkey Technology Team Foundation site will be all kinds barred from participation in events and activities.

- The issues to be considered in the language used in all communication with the TEKNOFEST Competitions Committee are as follows;
  - Rude and impolite words and behaviours should be avoided,
  - Insults, threats and bad words should be avoided,
  - E-mail, Facebook, Skype, Messenger, WhatsApp, Twitter etc. Avoid direct targeting and insulting with social media tools such as,
  - It is necessary to pay attention to the spelling rules and style in your petitions and objections.
- Situations, verbs, words etc. that will affect the functioning and motivation of other teams in the festival area. behaviour should not be exhibited.
- Social peace should be taken into consideration in the dormitory and its surroundings where accommodation services are provided. Otherwise, the initiation of the legal process against the person will be carried out by the relevant institutions.
- During the project and product development process, it is the responsibility of the team to back up / store the necessary equipment and materials in advance, taking into account all kinds of negativity, and to change parts in case of a possible negativity, and product supply from another team should not be provided.
- In the festival area and in all kinds of services provided by TEKNOFEST, it is necessary to pay attention to act in accordance with the service requirements in neutrality, without discrimination of language, religion, philosophical belief, political opinion, race, age and gender, without giving rise to behaviours and practices that prevent equal opportunity.
- It is necessary to pay attention not to use and use the goods and resources of TEKNOFEST and other companies-institutions-organizations other than their purposes and service requirements, and not to waste these goods and resources.
- It is necessary to support the activities carried out to facilitate the functioning of the festival, to meet its needs in the most effective, fast and efficient way, to increase the quality of service and to increase festival satisfaction.
- Competitors in the festival area to be careful about all kinds of benefits provided to themselves, their relatives, friends or persons or organizations with whom they are in contact and financial or other liabilities and similar personal interests that affect or seem to affect their performance in an impartial and objective manner. must take the necessary measures to avoid conflict of interest.
- In the use of TEKNOFEST, buildings and vehicles and other public goods and resources, it is necessary to avoid waste and waste, to act effectively, efficiently and economically when using working time, public goods, resources, labour and facilities.
- TEKNOFEST team members should be accountable for their responsibilities and liabilities and be open and ready for institutional evaluation and auditing, managers should take the necessary measures to prevent corruption with transactions or actions that are not in line with the objectives and policies of their institutions, and train their personnel on ethical principles of behaviour, this observe whether the principles are followed or not and guide in ethical behaviour.

- While performing their duties, team members should not make any statements, commitments, promises or attempts binding the institutions they work for, and should not make deceptive and unrealistic statements.

State of Responsibility

- T3 Foundation and TEKNOFEST are not responsible for any product delivered by the competitors or any injury or damage caused by the competitor. T3 Foundation and organization officials are not responsible for the damages caused by the competitors to third parties. T3 Foundation and TEKNOFEST are not responsible for ensuring that the teams prepare and implement their systems within the framework of the laws of the Republic of Turkey.

Turkey Technology Team Foundation reserves the right to make any changes in this specification.

APPENDIX

APP-1 Instructions to Be Supported

Table 4 : RV32I Basic Instruction Set

imm[31:12]				rd	0110111	LUI
imm[31:12]				rd	0010111	AUIPC
imm[20|10:1|11|19:12]				rd	1101111	JAL
imm[11:0]		rs1	000	rd	1100111	JALR
imm[12|10:5]	rs2	rs1	000	imm[4:1|11]	1100011	BEQ
imm[12|10:5]	rs2	rs1	001	imm[4:1|11]	1100011	BNE
imm[12|10:5]	rs2	rs1	100	imm[4:1|11]	1100011	BLT
imm[12|10:5]	rs2	rs1	101	imm[4:1|11]	1100011	BGE
imm[12|10:5]	rs2	rs1	110	imm[4:1|11]	1100011	BLTU
imm[12|10:5]	rs2	rs1	111	imm[4:1|11]	1100011	BGEU
imm[11:0]		rs1	000	rd	0000011	LB
imm[11:0]		rs1	001	rd	0000011	LH
imm[11:0]		rs1	010	rd	0000011	LW
imm[11:0]		rs1	100	rd	0000011	LBU
imm[11:0]		rs1	101	rd	0000011	LHU
imm[11:5]	rs2	rs1	000	imm[4:0]	0100011	SB
imm[11:5]	rs2	rs1	001	imm[4:0]	0100011	SH
imm[11:5]	rs2	rs1	010	imm[4:0]	0100011	SW
imm[11:0]		rs1	000	rd	0010011	ADDI
imm[11:0]		rs1	010	rd	0010011	SLTI
imm[11:0]		rs1	011	rd	0010011	SLTIU
imm[11:0]		rs1	100	rd	0010011	XORI
imm[11:0]		rs1	110	rd	0010011	ORI
imm[11:0]		rs1	111	rd	0010011	ANDI
0000000	shamt	rs1	001	rd	0010011	SLLI
0000000	shamt	rs1	101	rd	0010011	SRLI
0100000	shamt	rs1	101	rd	0010011	SRAI
0000000	rs2	rs1	000	rd	0110011	ADD
0100000	rs2	rs1	000	rd	0110011	SUB
0000000	rs2	rs1	001	rd	0110011	SLL
0000000	rs2	rs1	010	rd	0110011	SLT
0000000	rs2	rs1	011	rd	0110011	SLTU
0000000	rs2	rs1	100	rd	0110011	XOR
0000000	rs2	rs1	101	rd	0110011	SRL
0100000	rs2	rs1	101	rd	0110011	SRA
0000000	rs2	rs1	110	rd	0110011	OR
0000000	rs2	rs1	111	rd	0110011	AND

Table 5: RV64I Basic Instruction Set (in addition to RV32I)

imm[11:0]		rs1	110	rd	0000011	LWU
imm[11:0]		rs1	011	rd	0000011	LD
imm[11:5]	rs2	rs1	011	imm[4:0]	0100011	SD
000000	shamt	rs1	001	rd	0010011	SLLI
000000	shamt	rs1	101	rd	0010011	SRLI
010000	shamt	rs1	101	rd	0010011	SRAI
imm[11:0]		rs1	000	rd	0011011	ADDIW
0000000	shamt	rs1	001	rd	0011011	SLLIW
0000000	shamt	rs1	101	rd	0011011	SRLIW
0100000	shamt	rs1	101	rd	0011011	SRAIW
0000000	rs2	rs1	000	rd	0111011	ADDW
0100000	rs2	rs1	000	rd	0111011	SUBW
0000000	rs2	rs1	001	rd	0111011	SLLW
0000000	rs2	rs1	101	rd	0111011	SRLW
0100000	rs2	rs1	101	rd	0111011	SRAW

Table 6: RV32M Standard Instruction Set Extensions

0000001	rs2	rs1	000	rd	0110011	MUL
0000001	rs2	rs1	001	rd	0110011	MULH
0000001	rs2	rs1	010	rd	0110011	MULHSU
0000001	rs2	rs1	011	rd	0110011	MULHU
0000001	rs2	rs1	100	rd	0110011	DIV
0000001	rs2	rs1	101	rd	0110011	DIVU
0000001	rs2	rs1	110	rd	0110011	REM
0000001	rs2	rs1	111	rd	0110011	REMU

Table 7: RV64M Standard Instruction Set Extensions (in addition to RV32M)

0000001	rs2	rs1	000	rd	0111011	MULW
0000001	rs2	rs1	100	rd	0111011	DIVW
0000001	rs2	rs1	101	rd	0111011	DIVUW
0000001	rs2	rs1	110	rd	0111011	REMW
0000001	rs2	rs1	111	rd	0111011	REMUW

Table 8: RVC Standard Command Set Extensions 1. Quarter

15 14 13	12 11 10	9 8 7	6 5	4 3 2	1 0	
000	0			0	00	*Illegal instruction*
000	nzuimm[5:4|9:6|2|3]			rd′	00	C.ADDI4SPN *(RES, nzuimm=0)*
001	uimm[5:3]	rs1′	uimm[7:6]	rd′	00	C.FLD *(RV32/64)*
001	uimm[5:4|8]	rs1′	uimm[7:6]	rd′	00	C.LQ *(RV128)*
010	uimm[5:3]	rs1′	uimm[2|6]	rd′	00	C.LW
011	uimm[5:3]	rs1′	uimm[2|6]	rd′	00	C.FLW *(RV32)*
011	uimm[5:3]	rs1′	uimm[7:6]	rd′	00	C.LD *(RV64/128)*
100	—				00	*Reserved*
101	uimm[5:3]	rs1′	uimm[7:6]	rs2′	00	C.FSD *(RV32/64)*
101	uimm[5:4|8]	rs1′	uimm[7:6]	rs2′	00	C.SQ *(RV128)*
110	uimm[5:3]	rs1′	uimm[2|6]	rs2′	00	C.SW
111	uimm[5:3]	rs1′	uimm[2|6]	rs2′	00	C.FSW *(RV32)*
111	uimm[5:3]	rs1′	uimm[7:6]	rs2′	00	C.SD *(RV64/128)*

Table 9: RVC Standard Command Set Extensions 2. Quarter

000	nzimm[5]	0		nzimm[4:0]		01	C.NOP *(HINT, nzimm≠0)*
000	nzimm[5]	rs1/rd≠0		nzimm[4:0]		01	C.ADDI *(HINT, nzimm=0)*
001	imm[11|4|9:8|10|6|7|3:1|5]					01	C.JAL *(RV32)*
001	imm[5]	rs1/rd≠0		imm[4:0]		01	C.ADDIW *(RV64/128; RES, rd=0)*
010	imm[5]	rd≠0		imm[4:0]		01	C.LI *(HINT, rd=0)*
011	nzimm[9]	2		nzimm[4|6|8:7|5]		01	C.ADDI16SP *(RES, nzimm=0)*
011	nzimm[17]	rd≠{0, 2}		nzimm[16:12]		01	C.LUI *(RES, nzimm=0; HINT, rd=0)*
100	nzuimm[5]	00	rs1′/rd′	nzuimm[4:0]		01	C.SRLI *(RV32 NSE, nzuimm[5]=1)*
100	0	00	rs1′/rd′	0		01	C.SRLI64 *(RV128; RV32/64 HINT)*
100	nzuimm[5]	01	rs1′/rd′	nzuimm[4:0]		01	C.SRAI *(RV32 NSE, nzuimm[5]=1)*
100	0	01	rs1′/rd′	0		01	C.SRAI64 *(RV128; RV32/64 HINT)*
100	imm[5]	10	rs1′/rd′	imm[4:0]		01	C.ANDI
100	0	11	rs1′/rd′	00	rs2′	01	C.SUB
100	0	11	rs1′/rd′	01	rs2′	01	C.XOR
100	0	11	rs1′/rd′	10	rs2′	01	C.OR
100	0	11	rs1′/rd′	11	rs2′	01	C.AND
100	1	11	rs1′/rd′	00	rs2′	01	C.SUBW *(RV64/128; RV32 RES)*
100	1	11	rs1′/rd′	01	rs2′	01	C.ADDW *(RV64/128; RV32 RES)*
100	1	11	—	10	—	01	*Reserved*
100	1	11	—	11	—	01	*Reserved*
101	imm[11|4|9:8|10|6|7|3:1|5]					01	C.J
110	imm[8|4:3]	rs1′		imm[7:6|2:1|5]		01	C.BEQZ
111	imm[8|4:3]	rs1′		imm[7:6|2:1|5]		01	C.BNEZ

Table 10: RVC Standard Command Set Extensions 3. Quarter

000	nzuimm[5]	rs1/rd≠0	nzuimm[4:0]	10	C.SLLI *(HINT, rd=0; RV32 NSE, nzuimm[5]=1)*
000	0	rs1/rd≠0	0	10	C.SLLI64 *(RV128; RV32/64 HINT; HINT, rd=0)*
001	uimm[5]	rd	uimm[4:3|8:6]	10	C.FLDSP *(RV32/64)*
001	uimm[5]	rd≠0	uimm[4|9:6]	10	C.LQSP *(RV128; RES, rd=0)*
010	uimm[5]	rd≠0	uimm[4:2|7:6]	10	C.LWSP *(RES, rd=0)*
011	uimm[5]	rd	uimm[4:2|7:6]	10	C.FLWSP *(RV32)*
011	uimm[5]	rd≠0	uimm[4:3|8:6]	10	C.LDSP *(RV64/128; RES, rd=0)*
100	0	rs1≠0	0	10	C.JR *(RES, rs1=0)*
100	0	rd≠0	rs2≠0	10	C.MV *(HINT, rd=0)*
100	1	rs1≠0	0	10	C.JALR
100	1	rs1/rd≠0	rs2≠0	10	C.ADD *(HINT, rd=0)*
101	uimm[5:3|8:6]		rs2	10	C.FSDSP *(RV32/64)*
101	uimm[5:4|9:6]		rs2	10	C.SQSP *(RV128)*
110	uimm[5:2|7:6]		rs2	10	C.SWSP
111	uimm[5:2|7:6]		rs2	10	C.FSWSP *(RV32)*
111	uimm[5:3|8:6]		rs2	10	C.SDSP *(RV64/128)*

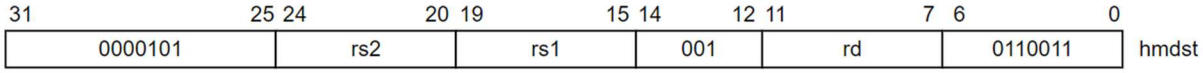
APP-2 Custom Instructions to be Supported

One of the key features of the RISC-V architecture is that it provides a foundation for application-specific instruction extensions. It can continue to provide software support for a design that has its own instructions outside of the main architecture, by offering instruction coding in different ways. In this way, instructions can be defined and executed to speed up a certain operation or to add an extra feature, using the space reserved for custom instructions.

The processors to be designed in the TEKNOFEST 2022 Chip Design Competition are expected to support the following commands, which are mostly used in cryptography algorithms:

hmdst

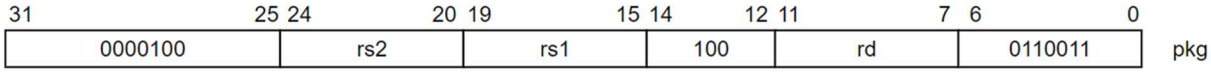
This instruction is used to calculate the Hamming distance of two 64-bit numbers. The instruction coding is as follows:



This instruction reads the rs1 and rs2 registers, it calculates the bit differences between them and writes it to the rd register.

pkg

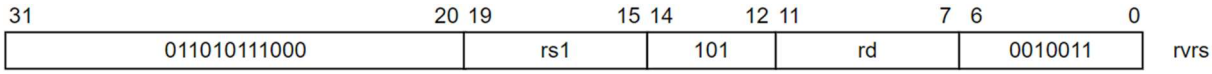
This command packs the least the significant half of the two registers and writes to another register. The instruction coding is as follows:



This instruction combines the least significant half of the values in the rs2 and rs1 registers and writes it to the rd register such that the half of rs2 remains in the most significant part.

rvrs

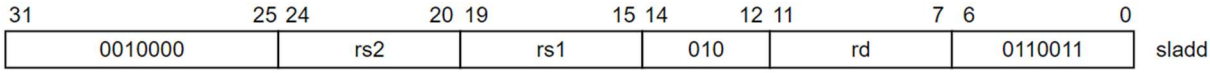
This instruction reverses the byte order of the value in a register. The instruction coding is as follows:



This instruction reads the rs register, reverses the byte order and writes it to the rd register.

sladd

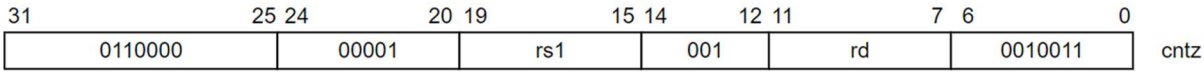
This instruction shifts the value in one register by one to the left and adds the value in another register. The instruction coding is as follows:



This instruction shifts the value in the rs1 register to the left by 1 bit, then sums it up with the value in rs2 and writes it to the rd register.

cntz

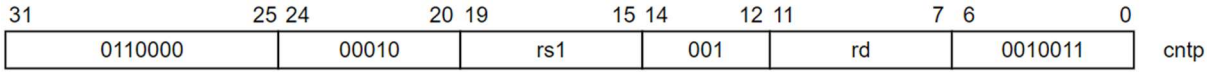
This instruction counts the trailing zeros of a value in a register. The instruction coding is as follows:



This instruction counts the number of 0s from the least significant bit to the most significant bit until a 1 and writes the result to the rd register. If the rs1 register is equal to 0, the result is XLEN, and if the least significant bit is 1, the result is equal to 0.

cntp

This instruction counts the number of ones in a register. The instruction coding is as follows:



It counts the number of ones in rs1 and writes the result to the rd register.

APP-3 Peripheral Details

Peripherals must be built with peripheral buses and devices that support the peripheral bus protocol. Any peripheral bus protocol can be chosen based on performance needs. One peripheral host and two devices must be supported.

It is desired to design two peripherals, Universal Asynchronous Receiver / Transmitter (UART) and Serial Peripheral Interface (SPI). A memory map should be created where peripheral controls will be carried out. Memory maps should be designed to require only 32-bit memory accesses. In order for your designs to integrate seamlessly on test systems, all the specifications for peripherals must be supported.

UART

In this section, the basic features of the UART device to be designed are specified.

The UART module should be a serial-to-parallel (rx) and parallel-to-serial (tx) full-dublex design, typically intended to communicate with an external device for terminal style communication. Programmable baud rate up to 1 Mbps must be guaranteed.

Features:

- 1 start bit, 8 data bits, no parity bit, 1 stop bit
- Programmable baud rate
- 32 x 8-bit rx buffer
- 32 x 8-bit tx buffer
- rx input port
- tx output port

Memory Map:
The memory map for the UART peripheral control registers is shown in Table x1.

Table 11: UART Memory Map

Address	Name	Description
0x20000000	uart_ctrl	Control Register
0x20000004	uart_status	Status Register
0x20000008	uart_rdata	Data Read Register
0x2000000c	uart_wdata	Data Write Register

UART Control Register

Controls the operation of the tx and rx channels.

Table 12: UART Control Register

uart_ctrl reset default: 0x0, mask: 0xFFFF0003			
Bits	**Type**	**Name**	**Description**
0	read / write	tx_en	tx enable
1	read / write	rx_en	rx enable
15:2			Unused space
31:16	read / write	baud_div	Baud rate control

tx_en should check if tx channel is enabled or not. When enabled, transmission should be performed if there is data in the tx buffer.
rx_en should check if the rx channel is enabled. When enabled, the incoming data should be kept in the rx buffer until the read operation takes place.

For both tx and rx channels, the baud rate must be specified with **baud_div**. The relationship between the input clock frequency and the baud should be established with the following equation.

$$f_{baud} = \frac{f_{clk}}{baud_div + 1}$$

Table x3 gives examples of division values to obtain a particular baud rate at a particular clock frequency.

Table 13: Example of baud rate calculation values

Clock (MHz)	Target Baud (Hz)	baud_div	Actual Baud (Hz)
500	31250	16000	31250
500	115200	4340	115207
500	250000	2000	250000
500	1843200	271	1845018

UART Status Register

This register gives information about the rx and tx buffer states.

Table 14: UART Status Register

uart_status reset default: 0xC, mask: 0xF			
Bits	**Type**	**Name**	**Description**
0	read only	tx_full	tx buffer is full
1	read only	rx_full	rx buffer is full
2	read only	tx_empty	tx buffer is empty
3	read only	rx_empty	rx buffer is empty

UART Data Read Register

The data received serially from the rx channel is read in parallel with this register. After rx_en is enabled, data must be stored in the rx buffer until read from this register.

Table 15: UART Data Read Register

uart_rdata reset default: 0x0, mask: 0xFF			
Bits	**Type**	**Name**	**Description**
7:0	read only	rdata	Data read

UART Data Write Register

The data to be transmitted over the tx channel is written to this register and serial transmission is performed. Data write requests should be stored in the tx buffer when tx_en is not enabled, and data should be transmitted when the channel is active.

Table 16: UART Write Data Register

uart_wdata reset default: 0x0, mask: 0xFF			
Bits	**Type**	**Name**	**Description**
7:0	write only	wdata	Data write

SPI

In this section, the basic features of the SPI device that is intended to be designed are specified.

The SPI peripheral interface is a very common synchronous serial interface for non-chip peripherals such as NOR flash devices, ADCs, DACs or temperature sensors. The interface is a de facto standard (not a formal one), so there is no definitive reference that defines the interface or sets the eligibility criteria. It is therefore important to make use of the datasheets of the desired peripheral devices to ensure compatibility. Devices to be used with the SPI interface within the scope of the competition will be shared with sample test codes.

Features:

- ➢ Support for all SPI polarity and phases modes
- ➢ Programmable SPI clock speed
- ➢ 8 x 32-bit miso buffer
- ➢ 8 x 32-bit mosi buffer
- ➢ miso input port
- ➢ sck, cs, mosi output port

Memory Map:
The memory map for the SPI peripheral control registers is shown in Table x7.

Table 17: SPI Memory Map

Address	Name	Description
0x20010000	spi_ctrl	Control Register
0x20010004	spi_status	Status Register
0x20010008	spi_rdata	Data Read Register
0x2001000c	spi_wdata	Data Write Register
0x20010010	spi_cmd	Command Register

SPI Control Register

Controls the operation of the serial transmit and receive channels.

Table 18: SPI Control Register

spi_ctrl reset default: 0x0, mask: 0xFFFF000F			
Bits	**Type**	**Name**	**Description**
0	read / write	spi_en	Enables the SPI
1	read / write	spi_rst	Resets the SPI
2	read / write	cpha	SPI clock phase
3	read / write	cpol	SPI clock polarity
15:4			Unused space
31:16	read / write	sck_div	sck control

With **spi_en** and **spi_rst** the spi interface is enabled or reset.

Four different spi modes can be set with **cpha** and **cpol**.

The sync clock speed is determined by **sck_div**. The relationship between the input clock frequency and the sck is given by the formula:

$$f_{sck} = \frac{f_{clk}}{2(sck_div + 1)}$$

SPI Status Register

This register gives information about miso and mosi buffer status.

Table 19: SPI Status Register

spi_status reset default: 0xC, mask: 0xF			
Bits	**Type**	**Name**	**Description**
0	read only	mosi_full	mosi buffer is full
1	read only	miso_full	miso buffer is full
2	read only	mosi_empty	mosi buffer is empty
3	read only	miso_empty	miso buffer is empty

SPI Data Read Register

The data received serially from the miso channel is read with this register. Data must be stored in the miso buffer until it is read from this register.

Table 20: SPI Data Read Register

spi_rdata reset default: 0x0, mask: 0xFFFFFFFF			
Bits	**Type**	**Name**	**Description**
31:0	read only	rdata	SPI data read

SPI Data Write Register

Data to be transmitted serially over the mosi channel is written to this register. It should be stored in the mosi buffer until the write requests are forwarded.

Table 21: SPI Data Write Register

spi_wdata N reset default: 0x0, mask: 0xFFFFFFFF			
Bits	**Type**	**Name**	**Description**
31:0	write only	wdata	SPI data write

SPI Command Register

The bidirectional working synchronization is controlled. After the request to this register, data transfers from the buffers should be carried out according to this command.

Table 22: SPI Command Register

spi_cmd reset default: 0x0, mask: 0x000033FF			
Bits	**Type**	**Name**	**Description**
8:0	read only	length	Transfer byte amount
9	read only	cs_active	Chip select active after transfer
13:12	read only	direction	Transfer direction

With **length**, the data transfer length and the number of bytes are determined.

If **cs_active** is "0", the chip select is raised immediately after transfer, if "1" the chip select is left low. This allows longer and more complete spi transfers to be achieved.

direction refers to the direction of the command. If "0", empty loop. “1” is just miso. “2” is just mosi.

For 32-bit data, bytes must be transferred in little-endian.

APP-4 Shuffling Format for Instruction and Data

For instructions and data, shuffling should be performed so that each byte enters one S-box. Rijndael's S-boxes will be used in the shuffling operation. In the table, the column is determined by the least significant 4 bits and the row by the most significant 4 bits. For example, the 0x12 value is converted to 0xc9, and 0x4326 value is converted to 0x1af7, and so on.

Table 23: S-box

	00	**01**	**02**	**03**	**04**	**05**	**06**	**07**	**08**	**09**	**0a**	**0b**	**0c**	**0d**	**0e**	**0f**
00	63	7c	77	7b	f2	6b	6f	c5	30	1	67	2b	fe	d7	ab	76
10	ca	82	c9	7d	fa	59	47	f0	ad	d4	a2	af	9c	a4	72	c0
20	b7	fd	93	26	36	3f	f7	cc	34	a5	e5	f1	71	d8	31	15
30	4	c7	23	c3	18	96	5	9a	7	12	80	e2	eb	27	b2	75
40	9	83	2c	1a	1b	6e	5a	a0	52	3b	d6	b3	29	e3	2f	84
50	53	d1	0	ed	20	fc	b1	5b	6a	cb	be	39	4a	4c	58	cf
60	d0	ef	aa	fb	43	4d	33	85	45	f9	2	7f	50	3c	9f	a8
70	51	a3	40	8f	92	9d	38	f5	bc	b6	da	21	10	ff	f3	d2
80	cd	0c	13	ec	5f	97	44	17	c4	a7	7e	3d	64	5d	19	73
90	60	81	4f	dc	22	2a	90	88	46	ee	b8	14	de	5e	0b	db
a0	e0	32	3a	0a	49	6	24	5c	c2	d3	ac	62	91	95	e4	79
b0	e7	c8	37	6d	8d	d5	4e	a9	6c	56	f4	ea	65	7a	ae	8
c0	ba	78	25	2e	1c	a6	b4	c6	e8	dd	74	1f	4b	bd	8b	8a
d0	70	3e	b5	66	48	3	f6	0e	61	35	57	b9	86	c1	1d	9e
e0	e1	f8	98	11	69	d9	8e	94	9b	1e	87	e9	ce	55	28	df
f0	8c	a1	89	0d	bf	e6	42	68	41	99	2d	0f	b0	54	bb	16

Scrambled data that in memory must be de-scrambled to its original state with an inverted S-box module before it can be used.

Table 24: Inverted S-box

	00	**01**	**02**	**03**	**04**	**05**	**06**	**07**	**08**	**09**	**0a**	**0b**	**0c**	**0d**	**0e**	**0f**
00	52	09	6a	d5	30	36	a5	38	bf	40	a3	9e	81	f3	d7	fb
10	7c	e3	39	82	9b	2f	ff	87	34	8e	43	44	c4	de	e9	cb
20	54	7b	94	32	a6	c2	23	3d	ee	4c	95	0b	42	fa	c3	4e
30	08	2e	a1	66	28	d9	24	b2	76	5b	a2	49	6d	8b	d1	25
40	72	f8	f6	64	86	68	98	16	d4	a4	5c	cc	5d	65	b6	92
50	6c	70	48	50	fd	ed	b9	da	5e	15	46	57	a7	8d	9d	84
60	90	d8	ab	00	8c	bc	d3	0a	f7	e4	58	05	b8	b3	45	06
70	d0	2c	1e	8f	ca	3f	0f	02	c1	af	bd	03	01	13	8a	6b
80	3a	91	11	41	4f	67	dc	ea	97	f2	cf	ce	f0	b4	e6	73
90	96	ac	74	22	e7	ad	35	85	e2	f9	37	e8	1c	75	df	6e
a0	47	f1	1a	71	1d	29	c5	89	6f	b7	62	0e	aa	18	be	1b
b0	fc	56	3e	4b	c6	d2	79	20	9a	db	c0	fe	78	cd	5a	f4
c0	1f	dd	a8	33	88	07	c7	31	b1	12	10	59	27	80	ec	5f
d0	60	51	7f	a9	19	b5	4a	0d	2d	e5	7a	9f	93	c9	9c	ef
e0	a0	e0	3b	4d	ae	2a	f5	b0	c8	eb	bb	3c	83	53	99	61
f0	17	2b	04	7e	ba	77	d6	26	e1	69	14	63	55	21	0c	7d

APP-5 Verilog RTL Writing Rules

In order to make the code easier to read and understand in the competition, the following guidelines should be followed.

- Each .v file should consist of a single module and the name of the file should be the same as the name of the module.
- Expressions such as always, if, else should start with begin and end with end.
- Indents should consist of 3 spaces.
- Clocks should start with clk. Additional attachments can be added upon request. eg; clk_memory.
- Resets should start with rst. Additional attachments can be added upon request. eg; rst_memory.
- The inside section in begin / end, module / endmodule, case / endcase should be indented from the previous section. Sample code is given below.

```
always @(posedge clk or negedge rst) begin
   if (!rsti) begin
     valid1 <= 1'b0;
   end else begin
     valid1 <= valid0;
   end
end
```

- Module inputs, outputs, and inouts should end with "_i", "_o", and "_io", respectively.
- Module expressions should be in Verilog-2001 format. After the "module" statement, the module name, input/output, signal should be in parentheses, and then the logic part of the module should be written. Sample code is given below.

```
module modul_ismi #(
  parameter int Size = 8
) (
  input                  clk_i,
  input                  rst_i,
  input   [Size-1:0]     rdata0_i,
  input   [Size-1:0]     rdata1_i,
  output [Size-1:0]   wdata0_o,
  output [Size-1:0]   wdata1_o
);
  …
endmodule
```

- When calling the module, it should not be called in a single line, but the parameters and the signal names should be written clearly one under the other. The unconnected input signal should be connected to ground and the unconnected output signal should be left blank. Sample code is given below.

```
  …
  modul_ismi #(
    . Size(16)
  ) örnek_isim (
    .clk_i (clk),
    .rst_i(1'b0), //unconnected empty input signal must be connected to the soil
    .rdata0_i (rdata) ,
    .rdata1_i (16'b0),//unconnected empty input signal must be connected to
the soil
    .wdata0_o (wdata),
    .wdata1_o () //unconnected idle output signal must be left blank
```

- When assigning two signals/ports to each other, the signal/port length should be the same. Automatic assignment should not be made.

```
wire [3:0] ornek_sinyal;
wire [6:0] ornek_sinyal2;
ornek_sinyal = 4'd4; = 4 gives the same, but the length is not the same.
ornek_sinyal2 = {3'b0,ornek_sinyal}; = ornek_sinyal gives the same, but the length is not the same.
```

- Combination blocks should only use blocking assignments (=).
- Sequential logic blocks should only use non-blocking assignments (<=).
- Signal names should be meaningful. Long and meaningful names should be preferred over short names.
- Comment lines should be added where necessary to clarify the code.