**TEKNOFEST**

**AEROSPACE AND TECHNOLOGY FESTIVAL**

**CHIP DESIGN COMPETITION**

**DIGITAL DESIGN CATEGORY**

**DETAILED DESIGN REPORT TEMPLATE**

**TEAM NAME**

**……………………………….**

**PROJECT NAME**

**………………………………**

**APPLICATION ID**

**………………………………**

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### DESIGN SUMMARY (5 POINTS)

{This section provides a summary of the activities carried out within the scope of the project.}

### PROJECT CURRENT STATUS ASSESSMENT (5 POINTS)

{In this section, the evaluation of the Preliminary Design Report is made. If any, the changes made after the preliminary design and why they were made are explained.}

### PROJECT DETAILED DESIGN (45 POINTS)

#### System Architecture

{In this section, the general block diagram of the final design is given and the compatibility of the system developed by competitors with the competition specifications is mentioned. Also, the algorithms/methods used in the final design are listed.}

#### Design Detail

##### Core Design

{The reasons for choosing all the blocks and algorithms used in the final core design, how they were implemented, and their detailed block diagrams are given. It should be mentioned which algorithms and blocks meet which requirements in the specification. In the core datapath design, the following should be explained; whether there will be a pipeline, if yes, how many stages there will be, how many instructions will be processed in a clock cycle, and the effects of features added to increase performance on all metrics. It should be explained how to optimally handle control-flow instructions such as branch and jump, whether to process instructions such as multiplication and division in a single cycle or in multiple cycles, and if in multiple cycles, how to process subsequent instructions.}

##### Memory Designs

{The reasons for choosing the final memory hierarchy design, how it was implemented, and detailed block diagrams are given. The 1st and 2nd level caches and the memory unit to be found outside the chip should be mentioned in detail. In cache design, the following should be mentioned; how the memory blocks will be implemented, the set-associativity in each cache, the replacement and the write policies, and the effects of all the choices on area and performance. Also, the time to fetch data from caches in the worst and the best cases should be shown mathematically. }

##### Peripheral Designs

{Design details of the final peripherals, memory map support, connection to the bus, why the bus protocol was chosen, and how it was implemented should be explained with detailed block diagrams. }

### CHIP DESIGN FLOW (20 POINTS)

{Which different programs are used in the chip design flow should be shown on the flow chart. The purpose of the programs used in the flow should be mentioned. The layout view of the design should be given. The customizations made in order to improve the power consumption, performance, and area usage in the flow should be mentioned. The problems encountered during the design process, both in design & tool software, and how these problems were solved should be mentioned (For example, the P & R program gave an error that it could not route the design, the competitors solved this situation with a method or an error was received during the flow, another version of the tool in newer commit was used to solve it). Theoretical, generally valid information used during these solutions should be included (For example, according to the information obtained from this source, the utilization value was kept below this value). If there are inconsistencies in the results obtained with the aforementioned general information due to the use of open-source programs, the reason for these should be explained. Power consumption, area usage, DRC/LVS/antenna results, setup hold timing reports, DRV (maximum capacitance, maximum fanout, maximum slew) reports as a result of flow should be mentioned. Although the design must pass the relevant checks at the TT (Typical-Typical) - 25°C - 1.80V corner, an explanation should be made about the situation in the other corners for the sake of completeness. If there are places such as communities and Slack channels that were used throughout the chip design flow, it should be mentioned which ones were used and in what way. It should be briefly mentioned which of the stages in the chip flow were easier and which were more difficult, and how much time was spent on which ones.}

### TEST (10 POINTS)

{In this section, it is explained how the processor will be tested in the FPGA implementation. The information about RTL level and post-layout simulation environment is given. It should be explained which test scenarios will be implemented. eg. cache tests, peripheral tests, shuffling tests, performance tests, post-layout tests.}

### TEAM ORGANIZATION (5 POINTS)

#### Team Organization

{In this section, information about the current team members and the advisor, if any, is given. (Name, surname, school, department, class)}

#### Distribution of Tasks

{In this section, information about the current team organization is given and the contributions of the team members in the works completed within the scope of DDR are indicated in detail.}

### BUSINESS PLAN AND RISK PLANNING (5 POINTS)

{In this part, time planning including the design, IC flow, and testing processes of the project and risk planning are given. It is clearly shown on the timing schedule, how many of the work packages were completed and how many of them have not been completed yet. It is mentioned whether there is any delay with respect to the schedule given in PDR.}

### REFERENCES (5 POINTS)

{This section should include the references used in the report. References should also be cited inside the report (So, the reader should know which part of the report was written in other words after taking particular reference as a basis.).}

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| **NOTE ON REPORT DRAFTS:** |
| **-All reports should be written in accordance with academic reporting standards.****- Information about the contents of the reports is stated above.****-All reports should include "Table of Contents" and "Bibliography".****-Each report should contain a cover page.****- Reports pages should be numbered consecutively.****-Font type: Calibri, Size: 11, Line Spacing: 1.15****-The report should have a maximum of 20 pages.** |